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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,664	04/14/2004	Hiroshi Akasaki	XA-9665A	4905

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
NGUYEN, VAN THU T	
ART UNIT	**PAPER NUMBER**
2824	

DATE MAILED: 10/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/823,664	AKASAKI ET AL.
	Examiner	Art Unit
	VanThu Nguyen	2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11 and 20-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11, 20-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10153525.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/14/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 11, 20-23 are pending.

2. Claims 1-10, 12-19 are cancelled.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: SEMICONDUCTOR INTEGRATED CIRCUIT HAVING PROGRAMMABLE DELAYS FOR GENERATING TIMING SIGNALS WITH TIME DIFFERENCE BEING NON-INTEGRAL MULTIPLE OF CLOCK CYCLE.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 11, 20-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 11, lines 10-12, it is not clear what apparently means in "the total of signal response periods of individual circuit blocks of the plurality circuit blocks is T2".

In claim 11, it is not clear if n on line 13 is same as that on line 16.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 11 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (U.S. Patent No. 6,125,064).

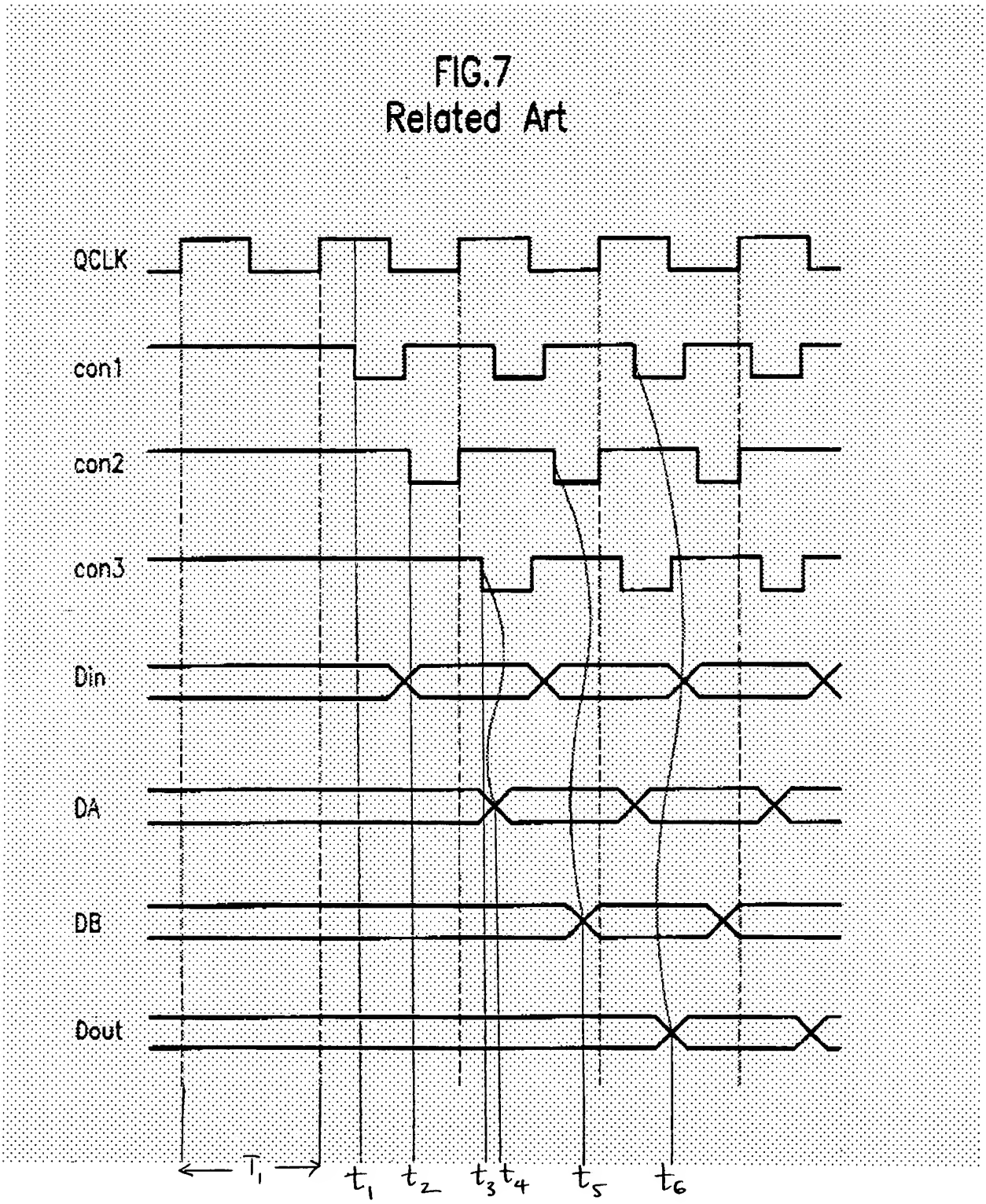
Regarding claim 11, Kim discloses, in FIG 1 and FIG. 7 illustrated below:

a semiconductor integrated circuit device which has a signal input point (for data input), a signal output point (for data output), and plural circuit blocks (first latch 2, second latch 3, and third latch 4) provided in series between the signal input point and the signal output point and in which the timings of a signal input operation from the signal input point, a signal output operation at the signal output point, and a signal transmission operation among the plural circuit blocks are respectively controlled by timing signals (timing signals con3, con2, and con1, respectively for each latch),

wherein, when the clock signal cycle is T1 (clock QCLK with cycle T1, see FIG. 7 below), the total of signal response periods of individual circuit blocks of the plural circuit blocks is T2 (adding up the time for: con1 (after 2nd dash line to time signal Dout responds, which is t1 to t6, approximately 2 ¼ T1) + con2 (after 2nd dash line to time signal DB responds, which is t2 to t5, approximately 1 1/6 T1) + con3 (after 3rd dash line to time signal DA responds, which is t3 to t4, approximately 1/9 T1) and the ratio T2/T1 between T1 and T2 is $n + \alpha$ (n is an integer and α is a positive number equal to or less than 1) (which is (2 ¼ T1 + 1 1/6 T1 + 1/9 T1) : T1 = 3 19/36, wherein n = 3 and α = 19/36), a signal response period from the signal input point to the signal output point is

set to n+1 times the clock signal cycle T1 (activation time of QCLK from 1st dash line to 5th dash line is 4T1, which is 3 + 1).

FIG.7
Related Art



Regarding claim 20, Kim further discloses wherein said plural circuit blocks include a first circuit block (first latch 2) and a second circuit block (second latch 3), wherein said first circuit block receives a signal input (Din) in accordance with a first timing signal (con3), wherein said second circuit block outputs a signal output (DA) in accordance with a second timing signal (con2), wherein said first and second timing signals are controlled by said clock signal (con3 and con2 are inherently derived from QCLK).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Weier et al. (U.S. Patent No. 6,108,266).

Regarding claim 21, Kim discloses a timing generating circuit (controlling circuit unit 1) which generates said first (con3) and second (con2) timing signals in accordance with said clock signal (QCLK); a plurality of inherent DRAM macro cells; inherent read and write buffers; and an address decoder.

However, Kim is silent about said timing generating circuit includes a delay circuit which is programmable.

Weier discloses a memory device comprising a programmable delay device 200 (see FIG. 2) having a plurality of predetermined delay blocks 202-205 in series, controlled by signals 220-

223; a plurality of SRAM cells in bit array 128 (see FIG. 1); read and write buffers 307 and 309 (see FIG. 3); row and column address decoders 126 and 130 (see FIG. 1).

Since Kim and Weier are both from the same field of endeavor, the purpose disclosed by Weier would have been recognized in the pertinent art of Kim.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art use programmable delay for the purpose of improving circuit performance (see column 1 lines 58-62).

Regarding claim 22, Kim also disclose wherein said time difference (t2 to t3, see illustrated FIG. 7 above) between said first (con3) and second (con2) timing signals is other than a multiple cycle of said clock signal (t2 to t3 is less than T1).

Regarding claim 23, Weier discloses the memory device further comprising a redundancy address setting circuit including fuses, and wherein said timing generating circuit includes fuses (see column 4, lines 9-32).

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (571) 272-1881. The examiner can normally be reached on Monday-Friday, 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

September 29, 2005

VanThu Nguyen
Primary Examiner
Art Unit 2824